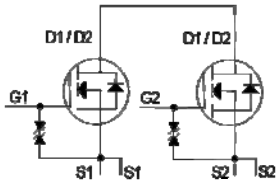
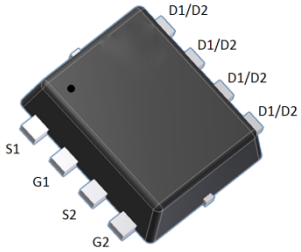
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	20V
$R_{DSON\ (MAX.)}$	14mΩ
I_D	9.5A





Pb-Free Lead Plating & Halogen Free

ESD Protection

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	9.5	A
	T_A = 70 °C		7.7	
Pulsed Drain Current[1]		I_{DM}	40	
Power Dissipation	T_A = 25 °C	P_D	2.1	W
	T_A = 70 °C		1.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient[3] (t≦10s)	$R_{\theta JA}$		60	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		105	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]The value of $R_{\theta JA}$ is measured with the device mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.35	0.65	1.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	9.5			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 5A		12.5	14	mΩ
		V_{GS} = 2.5V, I_D = 4A		14	17	
		V_{GS} = 1.8V, I_D = 3A		16	25	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5A		14		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		987		pF
Output Capacitance	C_{oss}			139		
Reverse Transfer Capacitance	C_{rss}			124		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		2.2		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 5A		15.1		nC
Gate-Source Charge[1,2]	Q_{gs}			1.1		
Gate-Drain Charge[1,2]	Q_{gd}			4.2		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			15		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			40		
Fall Time[1,2]	t_f			18		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				2	A
Pulsed Current[3]	I_{SM}				8	
Forward Voltage[1]	V_{SD}	I_F = 6A, V_{GS} = 0V		0.78	1.1	V

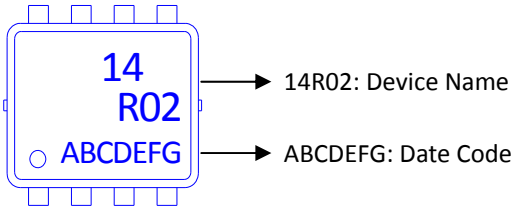
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

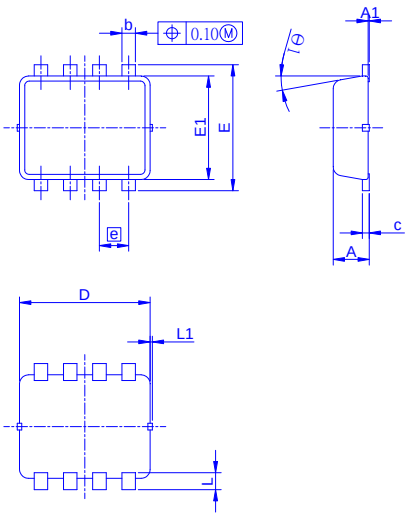
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB14N02BD for EDFN 3 x 3



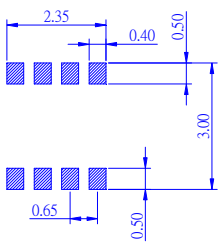
Outline Drawing



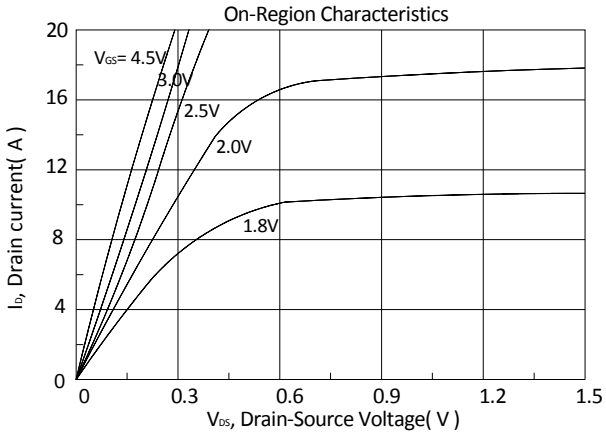
Dimension in mm

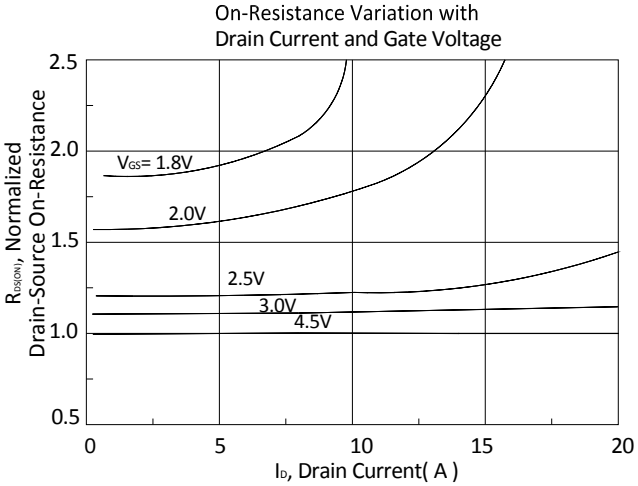
Dimension	A	A1	b	c	D	E	E1	e	L	L1	θ1
Min.	0.70	0	0.24	0.08					0.20	0	0°
Typ.	0.80		0.30	0.152	2.90	2.80	2.30	0.65	0.375		10°
Max.	0.90	0.05	0.35	0.25					0.45	0.10	12°

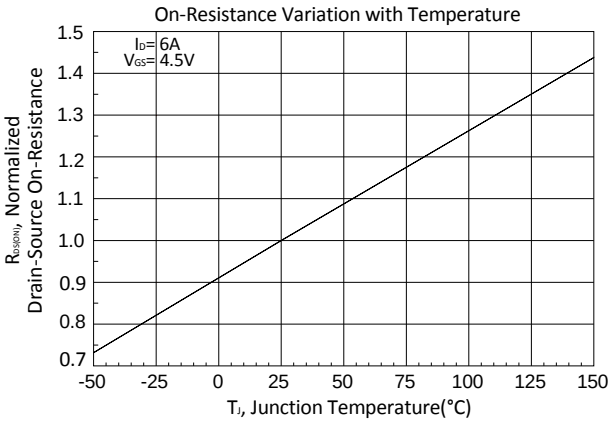
Recommended minimum pads

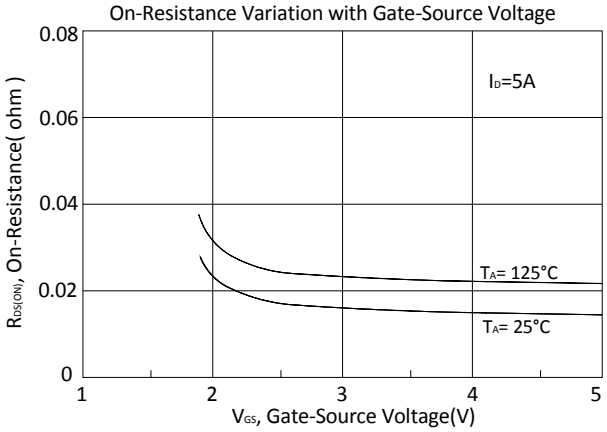


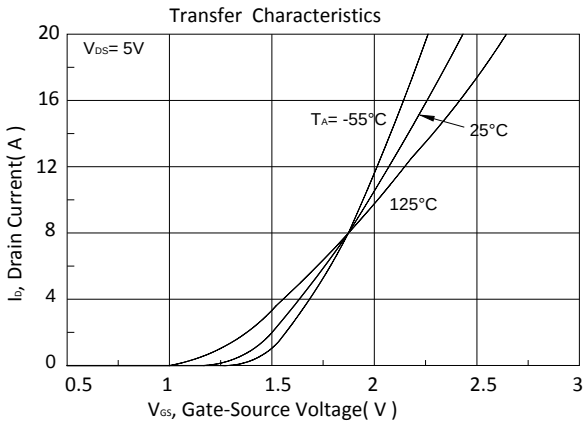
TYPICAL CHARACTERISTICS

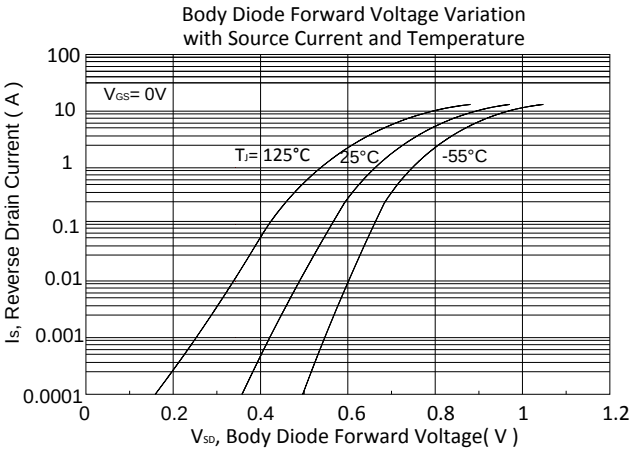


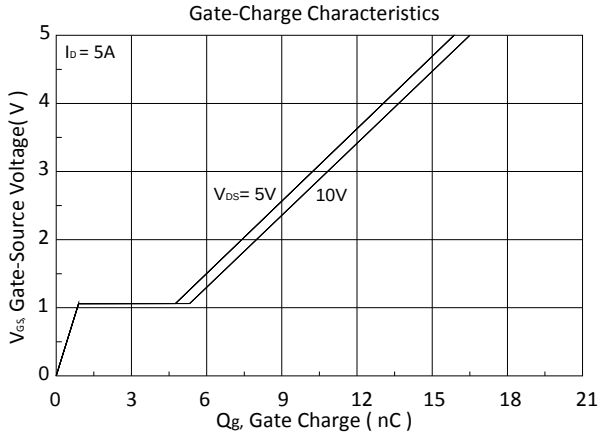


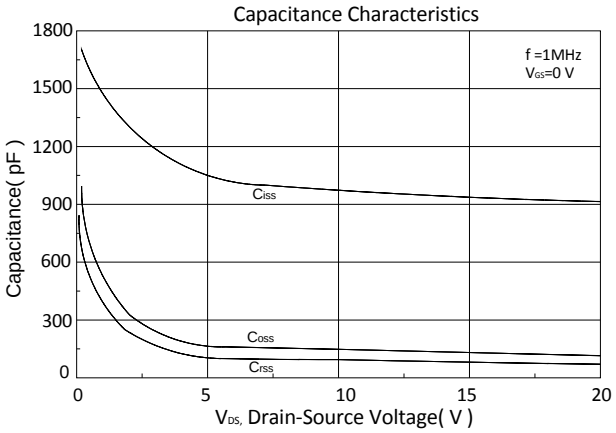


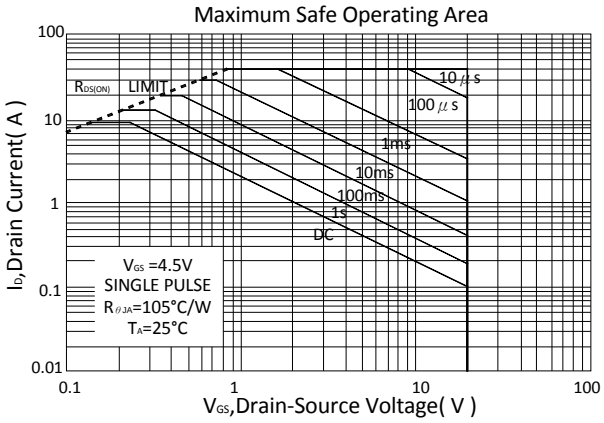


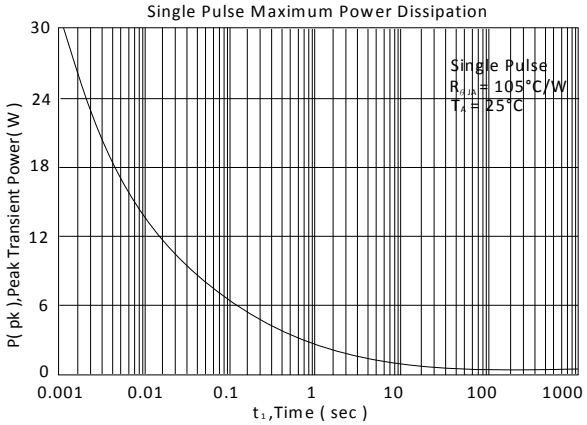


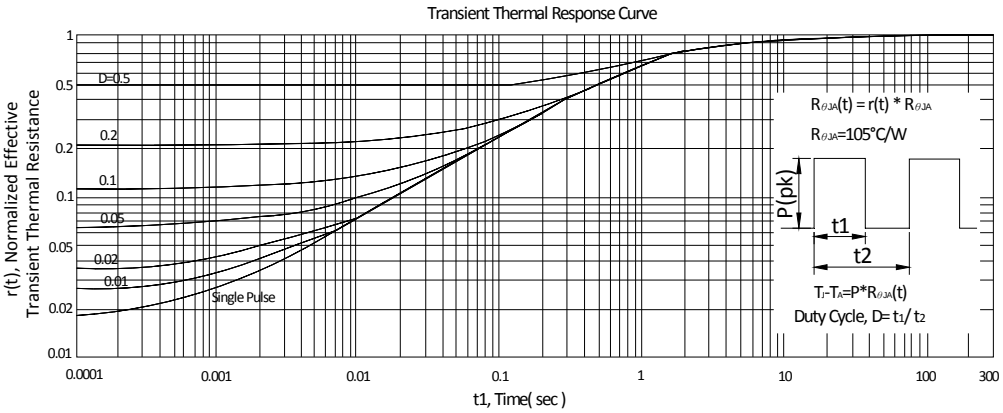



Gate-Charge Characteristics
I_D = 5A
V_{DS}= 5V
10V
V_{GS}, Gate-Source Voltage(V)
Qg, Gate Charge (nC)


Capacitance Characteristics
f =1MHz
V_{GS}=0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS}, Drain-Source Voltage(V)


Maximum Safe Operating Area
$R_{DS(ON)}$ LIMIT
10 μs
100 μs
1ms
10ms
100ms
1s
DC
V_{GS} =4.5V
SINGLE PULSE
$R_{\theta JA}$=105°C/W
T_A=25°C
I_D,Drain Current(A)
V_{GS},Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
$R_{\theta JA}$ = 105°C/W
T_A = 25°C
P(pk),Peak Transient Power(W)
t_1 ,Time (sec)


Transient Thermal Response Curve
D=0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
$R_{\theta JA}(t) = r(t) * R_{\theta JA}$
$R_{\theta JA}$=105°C/W
P(pk)
t1
t2
T_J-T_A=P*$R_{\theta JA}$(t)
Duty Cycle, D= t_1/ t_2
r(t), Normalized Effective Transient Thermal Resistance
t1, Time(sec)